

REMARKS

Claims 1-7 and 10-22 are pending in this application. Claims 8 and 9 are canceled. Claims 21-23 are new.

In the first Advisory Action mailed on April 1, 2008, the Examiner entered the amendment contained in the Amendment After Final filed by Applicants on March 11, 2008. In a second Advisory Action mailed on May 15, 2008, the Examiner indicated the Amendments After Final would not be entered. Applicants are filing the present RCE, in part, to ensure that the Amendments submitted on March 11, 2008, are of record for purposes of appeal. The redline in the amendments submitted herewith assumes entry of the Amendment After Final of March 11, 2008.

The Examiner rejected claims 1-20 under 35 U.S.C. Section 101 as directed to non-statutory subject matter and maintained this rejection in the Advisory Action. Applicants respectfully traverse the Examiner's rejections. Applicants will address each of the independent claims in turn. The dependent claims are directed to statutory subject matter by virtue of their dependencies.

With regard to independent claim 1, the Examiner contends that processing a digital signal is not a practical application. Claim 1 recites a method for processing a digital signal that is performed using a multiprocessor system, and which includes storing of the results of the process. In the words of the Federal Circuit, "claims in combining the use of machines with a mental process, claim statutory subject matter." *In re Comiskey*, 499 F.3d 1365, 1380 (Fed. Cir. 2007). To the extent the Examiner contends processing digital signals is not useful unless a particular application for the digital signal is recited, Applicants respectfully submit that digital signal processing is itself a commercially useful application, and when coupled with the use of a machine to perform the recited method of digital signal processing, and further with storage of the processed signal, is a tangible application. The Examiner's position that digital signal processing on a multiprocessor system is not a useful, tangible application is inconsistent with the reality of the marketplace, where tangible digital signal processing systems are regularly bought and sold and are highly useful. Further, claim 1 does not preempt every application of

the ideas because it is tied to use on a particular system, a multiprocessing system. Accordingly, claim 1 and the claims that depend therefrom are directed to statutory subject matter.

With regard to independent claim 3, the Examiner contends both that digital signal processing is not useful and that claim 3 is software “per se.” That digital signal processing is useful, and when tied to use on a system is a tangible application, is established above. Thus, claim 3, which recites “[a] linear scalable system to process a digital signal ... in a multiprocessing system,” is directed to statutory subject matter under *Comiskey*. Further, the Examiner’s reasoning that means-plus-function language that could be performed by a software module is not patentable is inconsistent with claim 3, which recites a multiprocessing system that would execute any such modules, and was rejected by *Comiskey*, which held that claims directed to software modules that require the use of a computer are directed to statutory subject matter. *Comiskey*, 499 F.3d at 1379. Accordingly, claim 3 and the claims that depend therefrom are directed to statutory subject matter. Further, dependent claims 4 and 15 recite memory locations in the means for storing inputs and outputs, and thus are directed to statutory subject matter for this additional reason.

With regard to independent claims 5 and 16, the Examiner contends a computer-readable memory medium is not tangible and that the claims do not indicate clearly that the code is intended to be executed on a computer system. The Examiner is incorrect on both points. The Federal Circuit has consistently explained that a claim which involves a mental process and one of the other categories of statutory subject matter may be directed to statutory subject matter. *Comiskey*, 499 F.3d at 1377 (listing cases). Independent claim 5 recites, “[a] computer program product comprising computer readable program code stored on a computer readable storage medium embodied therein for processing a digital signal ... in a multiprocessing system.” Independent claim 16 recites, “[a] computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal, the method comprising” Thus, claims 5 and 16 are directed to a useful application (signal processing) tied to another category of statutory subject matter (a composition, namely a computer-readable memory medium). See *Comiskey*, 499 F.3d at 1379 (dependent claims which tie the claimed process to “video [or radio], magnetic, electronic communication, or other

communications means” are directed to statutory subject matter) (citation omitted) (“[or radio]” in original). Both claims further indicate that the transformed signal is stored. Further, the claims indicate the computer-readable medium is intended for use in a processing system. Accordingly, claims 5 and 16 and the claims that depend respectively therefrom are directed to statutory subject matter.

The Examiner rejected claims 1-20 under 35 U.S.C. Section 103(a) as rendered obvious over U.S. Patent No. 5,991,787 issued to Abel, et al., in view of U.S. Patent No. 6,792,441 issued to Jaber. Applicants respectfully traverse the Examiner’s rejections.

Applicants previously argued that Abel was not an appropriate primary reference because the claims in the present application are directed to linearly scalable methods, systems and products for computing FFTs or inverse FFTs on multiprocessor systems, while Abel is directed to reducing peak spectral error for a specific processor, namely an MMXTM processor, using a specific instruction set and configuration. Abel reduces peak spectral error using rounding. Abel is not directed to linear scalability. Thus, the Examiner’s assertion that Abel discloses “a linear scalable method” is incorrect.

In the Advisory Action, the Examiner contends that the definition of linear scalability in the specification does not appear in the claims. The Federal Circuit has made it clear that a patentee may serve as its own lexicographer, and thus may define in the specification terms as used in the claims. *Sinorgchem Co. Shandong v. Int’l Trade Comm.*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) (“Our opinions have repeatedly encouraged claim drafters who choose to act as their own lexicographers to clearly define claim terms used in the claims in the specification) (holding International Trade Commission erred in ignoring portions of the definition of a claim term contained in the specification). Thus, the Examiner’s position that “linear scalable” will be giving no weight in the claims because the claims do not contain the definition set forth in the specification is an unreasonable interpretation of the claim language.

In the Final Office Action, the Examiner points to Figure 7 of Abel as disclosing linear scalability. Specifically, the Examiner contends Figure 7 shows “input coefficients can be any size.” Final Office Action, paragraph 8(a). The specification of the present application defines linear scalability as “the computation time reducing in inverse proportion to the number

of processors in the multiprocessor solution.” Specification at page 3, lines 11-14. Even assuming Figure 7 somehow shows that input coefficients can be any size (it does not, and the Examiner has failed to provide support for any argument that “input coefficients can be any size” is inherent in Figure 7), Figure 7 of Abel and the description thereof do not address linear scalability of a multi-processor system. Thus, Applicants continue to contend that Abel is not an appropriate primary reference because it does not address linear scalability. Further, Jaber is directed to specific hardware architectures, and is not directed to achieving linear scalability. Thus one would not be motivated to combine Abel and Jaber to obtain linear scalability in a multiprocessor system.

Further, the claimed invention uses a plurality of processors to perform a plurality of butterfly computations similar to the architecture claimed by Jaber. However, the present method does not necessitate the use of a “combination phase” used by Jaber, as shown in Fig 8 (component 817), Fig 9 (components 907, 909, 913A, 916 etc), Fig 10 right side, Fig 11 right side and Column 3 last paragraph. It is not obvious how the method outlined in the claims could be derived from Jaber’s teachings without use of the said combination phase.

Turning to the language of the claims, claim 1 recites, “[a] linear scalable method ... comprising ... computing an N-point FFT/IFFT of the signal using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix.” Claim 16 recites similar language. Neither Abel nor Jaber teach, suggest or motivate a linear scalable method comprising a first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix, as recited. Accordingly, claims 1 and 16 are not rendered obvious by Abel, alone or in combination with Jaber. Claims 2, 7, 10, 11 and 21 depend from claim 1 and claims 17-20 and 23 depend from claim 16, and are allowable at least by virtue of their dependencies.

Claim 3 recites, “[a] linear scalable system ... comprising: means for computing a plurality of stages of an N-point FFT/IFFT using in each stage of the plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop of a first radix and without employing nested loops.” Neither Abel nor Jaber teach, suggest or motivate a linear scalable system comprising: means for computing a plurality of stages of an N-point FFT/IFFT using in each stage of the plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop of a first radix and without employing nested loops, as recited. Accordingly, claim 3 is not rendered obvious by Abel, alone or in combination with Jabar. Claims 4, 12-15 and 22 depend from claim 3, and are allowable at least by virtue of their dependencies.

Claim 5 recites, “[a] computer program product ... for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time linear scalable approach, comprising: computer readable program code means configured for ... implementing the remaining ($\log_2 N - 2$) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops.” As mentioned above, neither Abel nor Jaber teach, suggest or motivate a linear scalable method. Thus, claim 5 is not rendered obvious by Abel, alone or in combination with Jaber. Claim 6 depends from claim 5 and is allowable at least by virtue of its dependency. Accordingly, claims 1-20 are not rendered obvious by Abel, alone or in combination with Jaber.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable.
Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
SEED Intellectual Property Law Group PLLC

A handwritten signature in dark ink, appearing to read 'Timothy L. Boller', is written over a horizontal line.

Timothy L. Boller
Registration No. 47,435

TLB:jms

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1183074_1.DOC